

Bigger
Faster
Wider

```
entity NOR2 is
  port (A, B: in BIT; Z: out BIT);
end NOR2;
architecture NOR2 of NOR2 is
begin
  P1: process (A, B)
    constant RISE_TIME: TIME:= 10 ns;
    constant FALL_TIME: TIME:= 8 ns;
    variable TEMP: BIT;
  begin
    TEMP:= A nor B
```



Lattice ispEXPERT™

Design Solutions for the Universe of ISP™ PLDs

ispEXPERT

Compiler and Design Systems

Introduction

Lattice's ispEXPERT™ compiler and design systems are Lattice's third-generation ISP design tools. They are new, powerful, and designed to improve user productivity and device performance. All the key features of world class design tools are included in a wide range of new products for Big, Fast, and Wide device design.

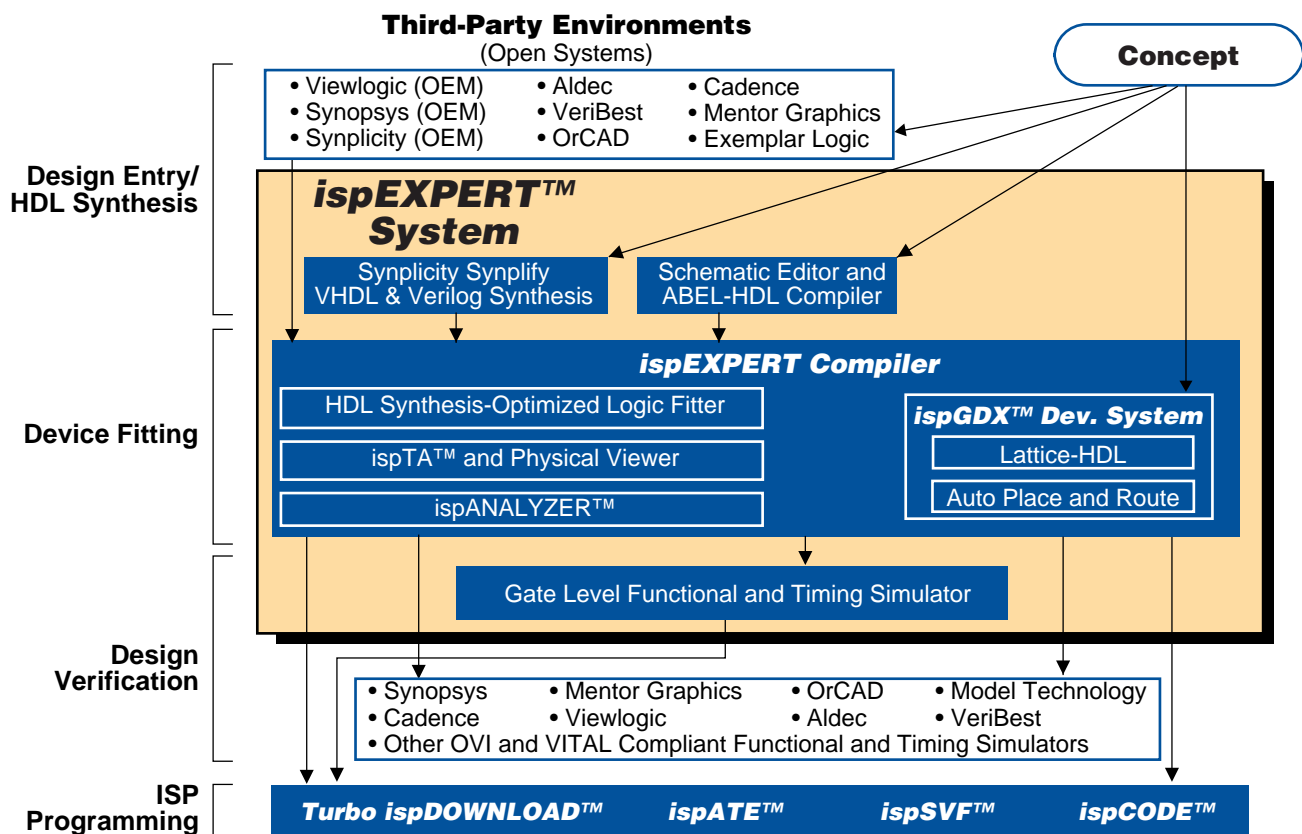
The ispEXPERT Compiler is the heart of these high performance tools. The Lattice compiler performs architecture-specific logic optimization, mapping, and place and route for all ispLSI devices and is a completely open system, accepting industry standard input and output formats.

The ispEXPERT System combines the Lattice compiler with a top-level Project Navigator, schematic editor, and ABEL®-HDL entry. The ispEXPERT System also includes Lattice's new gate-level functional and timing simulator, capable of simulating designs from VHDL, Verilog-HDL, ABEL and schematic source files.

Key Features

- VHDL and Verilog Synthesis
- Synplicity® - Synplify®
- Synopsys® - FPGA Express®
- Viewlogic® - Workview Office™
- Schematic Entry
- ABEL HDL Entry
- HDL Synthesis-Optimized Logic Compiler
- Architectural Synthesis
- Place & Route
- Project Navigator
- Explore Tool - Batch Processor
- Physical Viewer - Floorplan View
- Functional and Timing Simulation
- ispTA™ - Static Timing Analysis
- ispANALYZER™ - Hardware Debug Tool
- Integrated ISP Programming Tool
- Industry Standard Input / Output Formats

Lattice's ispEXPERT System Flow Diagram



ispEXPERT Power Tools

Lattice's vision is to provide users with efficient and effective design features like the ones shown here. New functions like the ispANALYZER, Timing Simulator and Physical Viewer

Explore Tool

Explore Tool – ispEXPERT tools include this unique feature for Compiler optimization. Using the Explore Tool's graphical user interface, engineers can set multiple system compilation controls in order to find the Compiler settings that are most efficient in processing their design for device speed and density.

- Fast optimization
- Easy to read spreadsheet display of results
- Smart Explore feature allows user to target desired results quickly.

Physical Viewer

The Lattice Physical Viewer speeds the process of determining silicon resource usage and optimization.

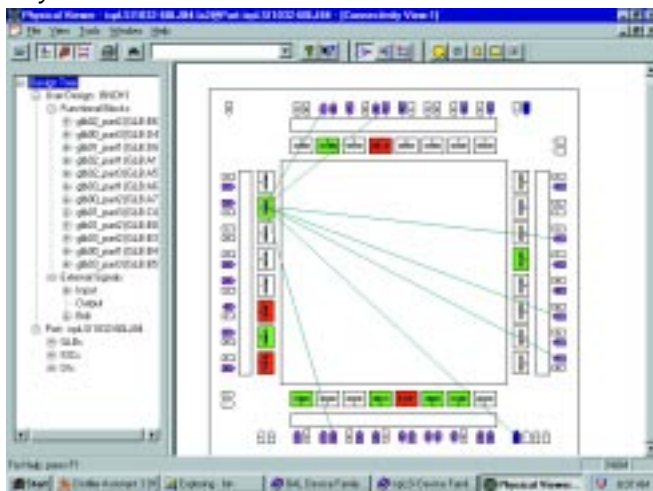
- Displays Functional Blocks and Resource Usage
- Graphical display of GLB, I/O Cell, and Dedicated Input Connections
- View Congestion and Unused Resources
- Displays Fan-In and Fan-Out Information
- Detailed Device Statistics

ispTA

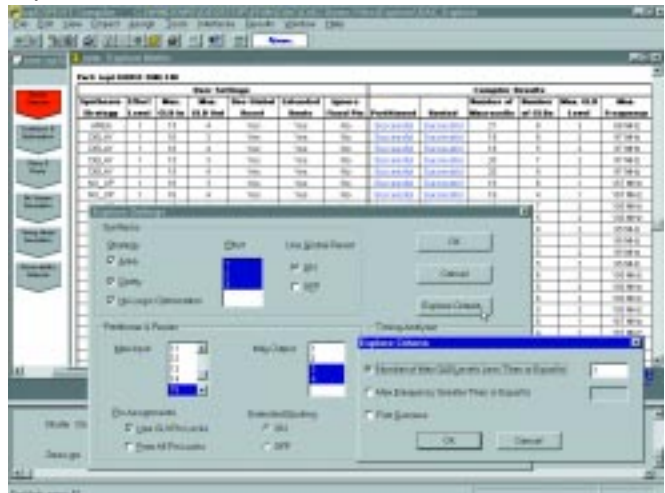
The ispEXPERT software has a built-in Static Timing Analyzer that provides accurate pin-to-pin timing information and allows the user to observe and evaluate design performance.

- Traces all signal paths and delays in an easy to read spreadsheet format
- Determines critical path information
- Evaluates maximum clock frequency

Physical Viewer



ispEXPLORE Tool



- Calculates chip boundary setup and hold requirements
- Calculates Tpd and Tco path delays
- Calculates GLB boundary delays
- Performs path enumeration

Lattice's Gate-Level Timing and Functional Simulator

Users can quickly and easily verify design logic and device timing through:

- Easy to use simulator control panel
- Simulation input flexibility – Supports VHDL, Verilog, Schematic and ABEL
- Simulation stimulus input – Waveform or ABEL test vector files
- Waveform Viewer for graphical results
- Back annotation to schematic

ispANALYZER

This tool is designed to speed the silicon debug process by providing complete access to buried functions. Without changing the logic design, an important distinction, a user may graphically connect observable functions to any unused pin.

- Graphical access to all observable buried registers/combinatorial functions
- Map user selected internal nodes to unused I/Os for hardware probing and test
- Incremental route to unused I/O pins without major redesign
- Creates JEDEC file and simulation model
- In-System program and verify observable configuration in seconds

ispCONNECTIONS™

Lattice also provides leading CAE vendor tools tightly integrated with the ispEXPERT System and ispEXPERT Compiler, and includes libraries to support design with all tools from leading 3rd-party CAE vendors.

ispEXPERT Compiler

Design entry is made simple by using software from leading third-party CAE vendors integrated with the ispEXPERT Compiler for design implementation. The Compiler offers high-level, device-independent design with efficient logic compilation, delivering unprecedented performance for the most complex designs. The ispEXPERT has been developed to operate efficiently in all third party environments and is optimized for high level Verilog and VHDL Synthesis and design.

ispEXPERT System with Synplicity

Lattice's ispEXPERT System with Synplicity, includes both VHDL and Verilog design synthesis through the easy-to-use Synplify synthesis engine. This complete system is packed with all the ispEXPERT System features and with powerful tools like Synplify Editing Window.

ispEXPERT Compiler with Viewlogic

The ispEXPERT Compiler with Viewlogic, is a complete design tool that includes Viewlogic's Workview Office System. VHDL and Verilog design synthesis, using Synopsys' FPGA Express software, is coupled with ViewDraw, ViewSim, and Viewlogic's Intelliflow project flow manager. Viewlogic's SpeedWave VHDL behavioral simulator is an option available for integration with the ispEXPERT Compiler with Viewlogic products.

ispEXPERT Packages and Interfaces

ispEXPERT Tools are available in a variety of configurations, including starter and base products, supporting up to 500 macrocell density device design and advanced products supporting all Lattice ispLSI devices, up to the new ispLSI 8840 device. The ispEXPERT tools support both PC and UNIX design platforms. ispEXPERT Synplicity and Viewlogic CAE solutions are available on the PC.

Lattice supports all the industry interfacing standards with EDIF 2.0.0 and 3.0.0, Standard Delay Format (SDF) 1.0 and 2.0, VITAL compliant VHDL, and OVI Compliant Verilog HDL. This provides a tight-integration with the tools in your existing design environment, and creates a complete ispLSI high-density programmable logic design solution.

ispCONNECTIONS Partners - Design Solutions Supported

ispCONNECTIONS Partner	Synthesis	Schematic	Compiler	Simulation	PC	Workstation
Aldec	✓	✓		✓	✓	
Cadence	✓	✓		✓		✓
Exemplar	✓				✓	✓
Mentor Graphics	✓	✓		✓		✓
Model Technology				✓	✓	✓
OrCAD	✓	✓	✓	✓	✓	
Synopsys	✓			✓	✓	✓
Synplicity	✓				✓	✓
Viewlogic	✓	✓	✓	✓	✓	✓
OVI Compliant Verilog				✓	✓	✓
VITAL Compliant HDL				✓	✓	✓



		Lattice ispEXPERT™ Design Tools						
		ispEXPERT System with Synplicity (Base)	ispEXPERT System with Synplicity (Advanced)	ispEXPERT Compiler with Viewlogic (Base)	ispEXPERT Compiler with Viewlogic (Advanced)	ispEXPERT Starter Software	ispEXPERT Compiler (Advanced) (PC)	ispEXPERT Compiler (Advanced) (WS)
Design Entry	Schematic	✓	✓	✓	✓	✓		
	ABEL	✓	✓			✓		
	VHDL	✓	✓	✓	✓			
	Verilog-HDL	✓	✓	✓	✓			
	CAE Vendor Libraries	✓	✓	✓	✓	✓	✓	✓
Logic Fitting	Timing Driven Synthesis & Fitting	✓	✓	✓	✓	✓	✓	✓
	Logic Synthesis & Fitting	✓	✓	✓	✓	✓	✓	✓
	Automatic Error Detection	✓	✓	✓	✓	✓	✓	✓
	Design Rule Checking	✓	✓	✓	✓	✓	✓	✓
	Flow Manager	✓	✓	✓	✓	✓		
Verification	ispTA	✓	✓	✓	✓	✓	✓	✓
	Functional Simulation	✓	✓	✓	✓	✓		
	Timing Simulation	✓	✓	✓	✓			
	Waveform Viewer	✓	✓	✓	✓			
	Explore Tool	✓	✓	✓	✓	✓	✓	✓
	Physical Viewer	✓	✓	✓	✓	✓	✓	✓
	ispANALYZER (Design Debugger)	✓	✓	✓	✓	✓	✓	✓
ISP Programming	ISP Daisy Chain Download	✓	✓	✓	✓	✓	✓	✓
	Turbo ispDOWNLOAD	✓	✓	✓	✓	✓	✓	✓
	ispJTAG Programming	✓	✓	✓	✓	✓	✓	✓
	ispATE	✓	✓	✓	✓	✓	✓	✓
	ispSVF	✓	✓	✓	✓	✓	✓	✓
	ispCODE	✓	✓	✓	✓	✓	✓	✓
Other	ispGAL/GAL Compiler	✓	✓			✓		
	On-Line Help	✓	✓	✓	✓	✓	✓	✓
	On-Line Documentation	✓	✓	✓	✓	✓	✓	✓
Device Support	ispLSI ≤500 Macrocells	✓		✓		✓		
	ispLSI – All		✓		✓		✓	✓
	ispGDX	✓	✓	✓	✓	✓	✓	✓
	ispGAL & GAL	✓	✓			✓		
	ispGDS	✓	✓	✓	✓	✓	✓	✓

Select the design tool which best fits your needs.

- Device Support – Choose from Starter/Base systems which support devices with up to 500 macrocells. Or select one of the Advanced systems which support all Lattice ispLSI devices.
- Third-Party Design Tools – Choose Synplicity or Synopsys/Viewlogic Design Tools from Lattice. Or the ispEXPERT Compiler which supports a wide variety of third-party CAE tools.
- Timing Simulation – Lattice offers a full gate-level functional and timing simulator with ispEXPERT System with Synplicity and ispEXPERT Compiler with Viewlogic. In addition, numerous third-party timing simulators and verification tools are supported by Lattice's ispEXPERT tools.

ISP Daisy Chain Download Programming

Lattice's ISP Daisy Chain Download Programming (ispDCD™) software is a powerful utility tightly integrated with the ispEXPERT Compiler and ispANALYZER software to

program any Lattice ISP Device. ispDCD supports either serial or parallel (Turbo ispDOWNLOAD) programming of all the Lattice devices in single or multiple ISP daisy chains. It supports mixed 3.3V and 5V devices, ISP and ispJTAG™ devices and even accepts non-Lattice devices in the same chain, with Boundary Scan test compatibility. Using the built-in ispATE capability users can generate an ispSTREAM™ for ATE programming.

ispATE™

Lattice's ISP Daisy Chain Download programming software includes an integrated facility to create Lattice specific ATE programming vectors for Genrad, Teradyne, Hewlett-Packard, and other ATE Systems. Through an easy-to-use graphical user interface vectors required to program and verify every Lattice ISP device on a board, at final test, are generated in the proper equipment format.

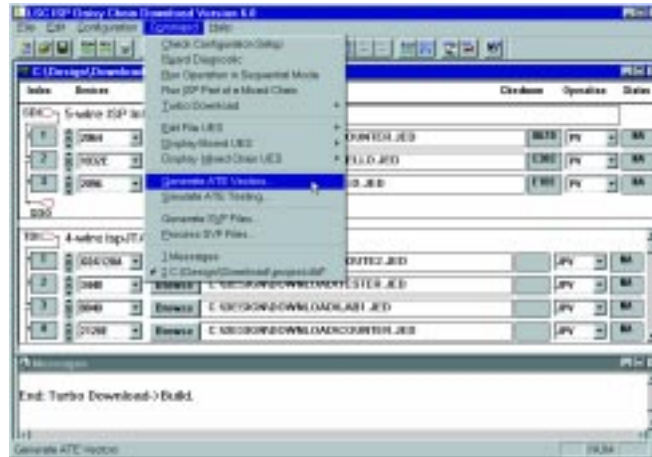
ispSVF™

Lattice supports the Serial Vector Format (SVF) language. SVF files, utilized primarily by ATE and boundary-scan based development tools, include both programming instructions and device data for single pass in-system programming. Additionally, ispSVF provides a vendor-independent file format that is seamlessly transportable across a wide array of programming hardware and test equipment. ispSVF files are easily generated from ISP Daisy Chain Download software.

ispCODE™

ispCODE consists of C source code routines for embedded programming of Lattice ISP devices. Integrate ispCODE into system software and program Lattice ispLSI devices from a system microcontroller or processor. ispCODE can be used to update hardware in the field, in remote locations, through phone lines or simple electronic means.

ISP Daisy Chain Download Programming Software



ispDOWNLOAD™ Cables

ISP programming can be performed from a PC or SUN workstation via a Lattice ispDOWNLOAD cable. The PC version connects to the PC parallel port and to the target PCB by an 8 pin AMP connector. The SUN version runs off a workstation serial port.

ispGDX™ Development System

Also included in the ispEXPERT packages is the windows-based ispGDX Development System, supporting Lattice's new series of in-system programmable Generic Digital Crosspoint devices. An easy-to-use hardware description language compiler combined with timing

simulation interfaces makes for a complete system for ispGDX device design.

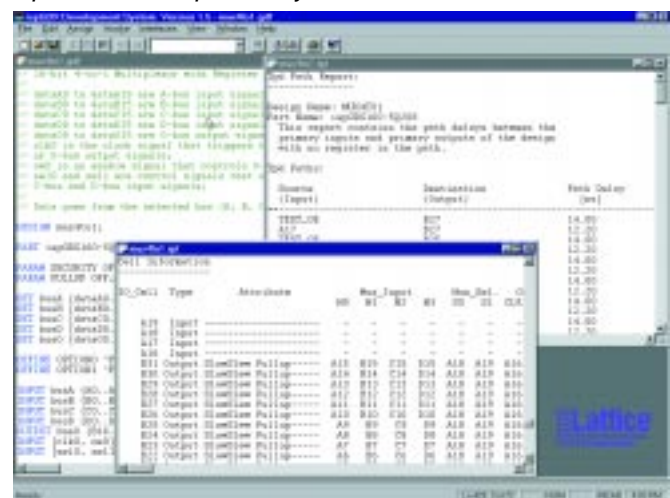
ispGDS™ Compiler

An easy to use ispGDS Compiler is included with every Lattice development tool. The compiler accepts a simple Lattice design language for design of all the ISP Generic Digital Switches.

ispGAL® and GAL® Compiler

The ispEXPERT Starter and ispEXPERT Systems with Synplicity include Lattice's ispGAL and GAL Compiler. Design any ispGAL or GAL device using the familiar ABEL-HDL language.

ispGDX Development System



ispEXPERT™ Design Tools Ordering Information

Product Name	Part #	Maintenance Part #	Maintenance Reinstatement Part #
ispEXPERT Compiler (Advanced) (PC)	EXPERT-CA	EXPERT-CAM	EXPERT-CAMR
ispEXPERT Compiler (Advanced) (PC) Floating License ADD-ON	EXPERT-CAF		
ispEXPERT Compiler (Upgrade) (PC)	EXPERT-CU		
ispEXPERT Compiler (Advanced) (WS)	EXPERT-CW	EXPERT-CWM	EXPERT-CWMR
ispEXPERT Compiler (Advanced) (WS) Floating License ADD-ON	EXPERT-CWF		
ispEXPERT Starter	FREE for download from the Lattice website (www.latticesemi.com)		
ispEXPERT System with Synplicity (Base)	EXPERT-SB	EXPERT-SBM	EXPERT-SBMR
ispEXPERT System with Synplicity (Advanced)	EXPERT-SA	EXPERT-SAM	EXPERT-SAMR
ispEXPERT System with Synplicity (Upgrade)	EXPERT-SU		
ispEXPERT Compiler with Viewlogic (Base)	EXPERT-VB	EXPERT-VBM	EXPERT-VBMR
ispEXPERT Compiler with Viewlogic (Advanced)	EXPERT-VA	EXPERT-VAM	EXPERT-VAMR
ispEXPERT Compiler with Viewlogic (Upgrade)	EXPERT-VU		
Viewlogic SpeedWave® VHDL Simulator	PDS3307-PC3	PDS3307M-PC3	PDS3307MR-PC3

Maintenance for Continued Support

Lattice Semiconductor Corp. offers maintenance coverage for continued device and feature support for all software systems. Diligently purchasing this annual coverage delivers significant benefits such as those delivered by the ispEXPERT tools:

The latest features to keep you ahead of your competition in designing and delivering products:

- Timing Simulator
- Physical Viewer
- ispANALYZER – In-System Debugging Tool
- 3rd Party Design Tool Enhancements

New Device Support

- ispLSI 2000E Family
- ispLSI 5000V Family
- ispLSI 8000 Family

The latest Programming, Platform, and Innovative Architecture releases

- ispGDx Development System supporting in-system programmable Generic Digital Crosspoint devices.
- ispDCD, supporting Turbo Download, ispATE, ispSVF, and ispCODE utilities.
- Operating system support and updates for Windows95, WindowsNT and UNIX platforms.

Our commitment is to provide the customer with the best tool set available. Contact your local Lattice authorized sales representative NOW!

System Requirements (PC Platform)

- 486/Pentium IBM Compatible PC
- Operating System
 - Windows NT®
 - Windows 95®
 - Windows 98®
- 32MB RAM with 150MB Hard Disk Space
- Parallel Printer Port for Software Key

Warranty/Update Service

- 90-day Warranty on Disc Material
- One-year Maintenance Support Included with Purchase
- Annual Maintenance Agreement Available

Technical Support

Hotline: 1-800-LATTICE (US and Canada)
1-408-428-6414 (International)
FAX: 1-408-944-8450
E-mail: ispLSlapps@latticesemi.com

Programming Adapters

Socket Adapter Part Number	Description	Package Identifier	Devices Supported	Sample Included
pDS4102-J44	44-Pin PLCC	LJ	ispLSI 1016E, 2032, 2032E, 2032V, 2064V	ispLSI 2032-80LJ
pDS4102-T44	44-Pin TQFP	LT	ispLSI 1016, 1016E, 2032, 2032E, 2032V, 2064V	ispLSI 2032-80LT
pDS4102-T48	48-Pin TQFP	LT48	ispLSI 2032, 2032E	ispLSI 2032-80LT48
pDS4102-J68	68-Pin PLCC	LJ	ispLSI 1024	ispLSI 1024-60LJ
pDS4102-J84	84-Pin PLCC	LJ	ispLSI 1032E, 2064	ispLSI 2064-80LJ
pDS4102-J84/2064V	84-Pin PLCC for 2064V	LJ	ispLSI 2064V, 2128V	ispLSI 2064V-60LJ84
pDS4102-T100	100-Pin TQFP	LT	ispLSI 1032E, 2064	ispLSI 2064-80LT
pDS4102-T100/1024	100-Pin TQFP for 1024	LT	ispLSI 1024	ispLSI 1024-60LT
pDS4102-T100/2128V	100-Pin TQFP for 2128V	LT100	ispLSI 2064V, 2128V	ispLSI 2128V-60LT100
pDS4102-Q128	128-Pin PQFP	LQ	ispLSI 1048E, 2096	ispLSI 2096-80LQ
pDS4102-Q128/2096V	128-Pin PQFP for 2096V	LQ128	ispLSI 2096V	ispLSI 2096V-60LQ128
pDS4102-T128	128-Pin TQFP	LT	ispLSI 1048E, 2096	ispLSI 2096-80LT
pDS4102-T128/2096V	128-Pin TQFP for 2096V	LT128	ispLSI 2096V	ispLSI 2096V-60LT128
pDS4102-Q160/2128V	160-Pin PQFP for 2128V	LQ160	ispLSI 2128V	ispLSI 2128V-60LQ160
pDS4102-T176	176-Pin TQFP	LT	ispLSI 2128, 2128E	ispLSI 2128-80LT
pDS4102-T176/2128V	176-Pin TQFP for 2128V	LT176	ispLSI 2128V	ispLSI 2128V-60LT176
pDS4102-T176/GX120	176-Pin TQFP for GDGX120A	T176	ispGDGX120A	ispGDGX120A-7T176
pDS4102-M208	208-Pin MQUAD	LM	ispLSI 6192SM, 6192DM, 6192FF	ispLSI 6192SM-50LM
pDS4102-M208/3320	208-Pin MQUAD for 3320	LM and LQ	ispLSI 3320	ispLSI 3160-70LQ
pDS4102-Q208	208-Pin PQFP	Q208	ispGDGX160	ispGDGX 160-7Q208
pDS4102-M240	240-Pin MQUAD	LM	ispLSI 3192	ispLSI 3192-70LM
pDS4102-M304	304-Pin MQUAD	LM	ispLSI 3256E	ispLSI 3256E-70LM

Hardware Programming Support

ISP Engineering Kit Model 100

The ISP Engineering Kit Model 100 is an engineering programmer that supports prototype development by allowing designers to program ispLSI devices directly from a PC. Together with the ispDCD software, the ISP Engineering Kit supports programming of single or multiple daisy-chained devices. The ISP Engineering Kit can be used as a stand-alone programmer or to directly download to an ispLSI device on a board. The kit accelerates the system and board level debug process and permits final board definition earlier in the design cycle.

Included in the kit is a programming module, ispDOWNLOAD cables and a 110V AC/9V DC power supply converter (for North America only). Socket adapters are purchased separately and are available for ispLSI package options. Each socket adapter comes with a sample of a corresponding ispLSI device so users can begin to program devices immediately.

ISP Manufacturing Kit

The ISP Manufacturing Kit is designed to aid the integration of Lattice ISP devices into the manufacturing environment. This tool includes all the software and hardware needed to fully integrate and debug in-system programming in a manufacturing environment using ATE equipment. It includes an ispDOWNLOAD cable and a unique ISP Manufacturing Board to allow engineers to fully evaluate and integrate ISP quickly.

This tool can be used in manufacturing and test to prototype and demonstrate ISP programming with ATE and debug test flows with ISP devices. With Lattice's ispLSI development tools and the ISP Manufacturing Kit, parallel development between design and test can be accomplished.

Ordering Information

Hardware Description

ISP Eng. Kit Model 100 (N. Amer./Asia)
 ISP Eng. Kit Model 100 (Europe)
 3.3V-to-5V Adapter for ISP Eng. Kit
 ispDOWNLOAD Cable (PC)
 ispDOWNLOAD Cable (Workstation)
 ISP Manufacturing Kit

Part Number

pDS4102-PM
 pDS4102E-PM
 pDS4102-3/5ADP
 pDS4102-DL2
 pDS4102-WS
 ISP-MFG1



5555 Northeast Moore Court
 Hillsboro, Oregon 97124-6421 U.S.A.

Telephone: (503) 681-0118

Internet: <http://www.latticesemi.com>

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